FM1110

Nonvolatile 5V Quad State Saver

Features

Nonvolatile State Saver

- Logic States Retained in Absence of Power
- Outputs Automatically Restored at Power-up
- Number of State Changes: 10^{12}
- Max t_{PD} 50ns at 4.5V
- Max Frequency 1 MHz

Low Power Operation

- Supply voltage of 4.5V to 5.5V
- 30 µA Standby Current

Industry Standard Configuration

- Industrial Temperature -40° C to +85° C
- 16-pin "Green"/RoHS QFN Package

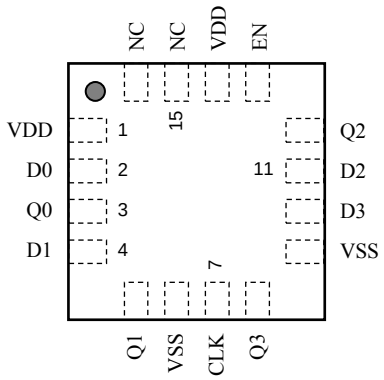
Overview

The FM1110 is an innovative FRAM-based device that stores inputs like conventional logic and retains the stored state in the absence of power. This product solves three basic problems in an elegant fashion. First, it provides continuous access to nonvolatile system settings without performing a memory read operation or using dedicated processor I/O pins. Second, it allows the storage of signals that may change frequently and possibly without notice. Third, it allows the nonvolatile storage of a system setting without the system overhead and extra pins of a serial memory.

Functionally, the inputs are stored and passed to the output on the rising edge of the clock CLK. This unique product serves a variety of applications. Here are a few applications:

- Control relays or valves with automatic setting on power-up without processor intervention
- Interface to soft/momentary front-panel switch and indicator lamp. Capture switch settings and drive LEDs without processor intervention
- Replaces jumpers & control signal routing
- Initialize state of I/O card signals
- Eliminate the overhead of serial memory for systems needing only a bit of data

Pin Configuration



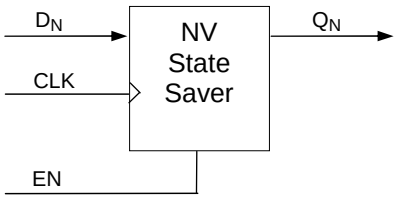
Top View

Pin Names	Function
D_N	Data In
Q_N	Data Out
EN	Enable
CLK	Clock
VDD	Supply Voltage
VSS	Ground

Ordering Information	
FM1110-QG	Quad State Saver, 16-pin "Green"/RoHS QFN

Ramtron International Corporation
1850 Ramtron Drive, Colorado Springs, CO 80921
(800) 545-FRAM, (719) 481-7000
http://www.ramtron.com

Block Diagram and Truth Table



INPUTS			OUTPUT
EN	**CLK**	**D_N**	**Q_N**
H	↑	L	L
H	↑	H	H
H	H or L	X	Q_0
L	X	X	Hi-Z

L Low voltage level
H High voltage level
X Don't Care
↑ CLK rising edge
Q_0 Previous output state before CLK ↑

Pin Descriptions

Pin Name	I/O	Description
D(3:0)	I	Data inputs
Q(3:0)	O	Data outputs
CLK	I	Clock: On a rising edge of CLK, the D_N inputs are transferred to the Q_N outputs. While CLK is high or low, the Q_N outputs do not change regardless of the state of the data inputs. See truth table.
EN	I	Enable. This active-high input enables the device. When low, inputs are ignored and updates to the nonvolatile cells are prevented. When high, the device operates normally.
VDD	Supply	Power Supply (4.5V to 5.5V)
VSS	Supply	Ground

Description

Nonvolatile storage applied to logic is a revolutionary concept. The FM1110 simplifies the design of system control functions. This product is unique because it remembers the stored output values in the absence of power. Any change in the latched state is automatically written to a nonvolatile ferroelectric latch. This function is possible due to the fast write time and extremely high write endurance of the underlying ferroelectric memory technology.

Use of Enable Pin

The FM1110 has an enable pin that is intended to be used in conjunction with a system reset. An active-low reset may be tied directly to the EN pin. At power-up, /RESET will be held low for some time during which the data input and CLK pins will be ignored. Once the system comes out of reset and EN goes high, the outputs Q_N drive to the state that were previously latched and the device operates normally. When the EN pin is low, the outputs Q_N are tri-stated.

The enable pin may be tied to V_{DD} since the device integrates a power management circuit that monitors the V_{DD} level during power cycles.

Electrical Specifications

Absolute Maximum Ratings

Symbol	Description	Ratings
V_{DD}	Power Supply Voltage with respect to V_{SS}	-1.0V to +7.0V
V_{IN}	Voltage on any signal pin with respect to V_{SS}	-1.0V to +7.0V and $V_{IN} < V_{DD}$+1.0V
T_{STG}	Storage temperature	-55°C to + 125°C
T_{LEAD}	Lead temperature (Soldering, 10 seconds)	300° C
V_{ESD}	Electrostatic Discharge Voltage - Human Body Model (JEDEC Std JESD22-A114-B) - Charged Device Model (JEDEC Std JESD22-C101-A) - Machine Model (JEDEC Std JESD22-A115-A)	 TBD TBD TBD
	Package Moisture Sensitivity Level	TBD

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and the functional operation of the device at these or any other conditions above those listed in the operational section of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

DC Operating Conditions (T_A = -40° C to + 85° C, V_{DD} = 4.5V to 5.5V unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V	
I_{SB}	Standby Current		-	30	µA	1
C_{PD}	Power Dissipation Capacitance		-	330	pF	2
I_{LI}	Input Leakage Current			±1	µA	3
I_{LO}	Output Leakage Current			±1	µA	3
V_{IL}	Input Low Voltage	-0.3		0.3 V_{DD}	V	
V_{IH}	Input High Voltage	0.7 V_{DD}		V_{DD} + 0.3	V	
V_{OH}	Output High Voltage @ I_{OH} = -1 mA	 V_{DD} – 0.5		 -	 V	
V_{OL}	Output Low Voltage @ I_{OL} = 1 mA (V_{DD}=4.5V) @ I_{OL} = 10 mA (V_{DD}=4.5V)	 - -		 0.4 0.8	 V V	
V_{HYS}	Input Hysteresis (CLK, EN)	150			mV	4

Notes

1. CLK = V_{SS}, all other inputs at V_{DD} or V_{SS}.
2. To calculate device power dissipation, $P_D = C_{PD}*V_{DD}^2*f_i + C_L*V_{DD}^2*f_o$, where f_i is the input clk freq, f_o is the output freq, and C_L is the output load capacitance. Active current I_{DD} may be calculated as $I_{DD} = C_{PD}*V_{DD}*f_i$, assuming outputs are floating.
3. V_{IN} or V_{OUT} = V_{SS} to V_{DD}.
4. This parameter is characterized but not tested.

AC Parameters (T_A = -40° C to + 85° C, V_{DD} = 4.5V to 5.5V, C_L = 30 pF unless otherwise specified)

Symbol	Parameter	Min	Max	Units	Notes
f_{MAX}	Maximum Clock Frequency		1	MHz	
t_{LOW}	CLK Low Period	0.3		µs	
t_{HIGH}	CLK High Period	0.3		µs	
t_{PD}	Propagation delay CLK to Q_N		50	ns	
t_{HZ}	EN Low to Q_N Hi-Z		25	ns	1
t_R	Input Rise Time		100	ns	1
t_F	Input Fall Time		100	ns	1
t_{DS}	Data (D_N) Setup Time to CLK ↑	5		ns	
t_{DH}	Data (D_N) Hold Time after CLK ↑	10		ns	
t_{EHD}	EN Hold Time (EN High after CLK ↑)	50	-	ns	
t_{EH}	EN High Time	5		µs	
t_{EL}	EN Low Time	2		µs	

Notes

1. This parameter is characterized but not tested.

Power Cycling and Data Retention (T_A = -40° C to + 85° C, V_{DD} = 4.5V to 5.5V, unless otherwise specified)

Symbol	Parameter	Min	Max	Units	Notes
	Nonvolatile Data Retention Time	45	-	years	
t_{VDR}	V_{DD} Rise Time	25	-	µs/V	1
t_{VDF}	V_{DD} Fall Time	50	-	µs/V	1
t_{RES}	EN High to Q_N Restore Time	-	0.5	µs	2
t_{PDS}	EN Low to Power Down Time	1	-	µs	
t_{EHFC}	EN High to First Clock (CLK ↑) after Power Up	4	-	µs	3

Notes

1. Slope measured at any point on V_{DD} waveform.
2. After power up, when EN goes high the nonvolatile latches are read and the values restored to the outputs Q_N.
3. After power up, this is the minimum time required before a state change operation may occur. EN and V_{DD} may be coincident at power up, and in this case t_{EHFC} time is referenced to V_{DD} (min) and CLK ↑.

Capacitance (T_A = 25° C , f=1.0 MHz, V_{DD} = 5.0V)

Symbol	Parameter	Min	Max	Units	Notes
C_I	Input Capacitance	-	14	pF	1

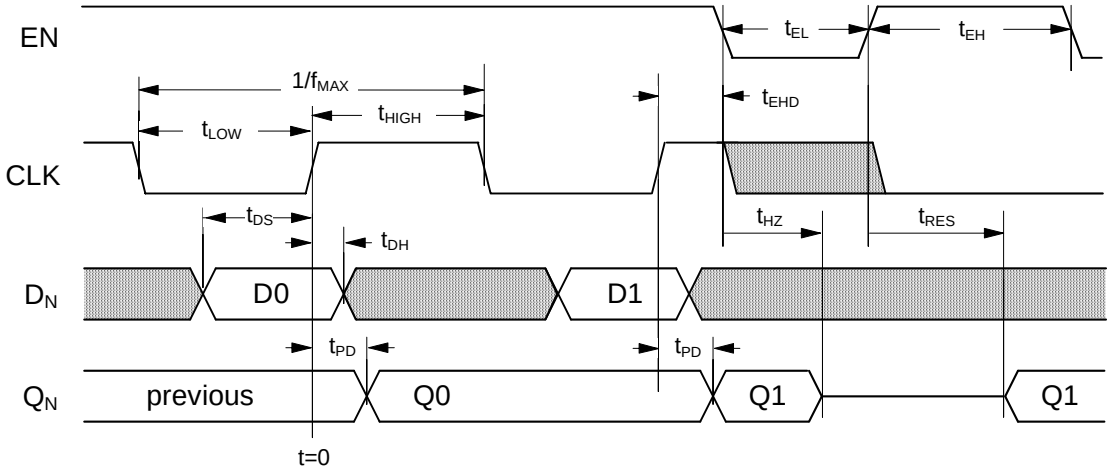
Notes

1. This parameter is characterized but not tested.

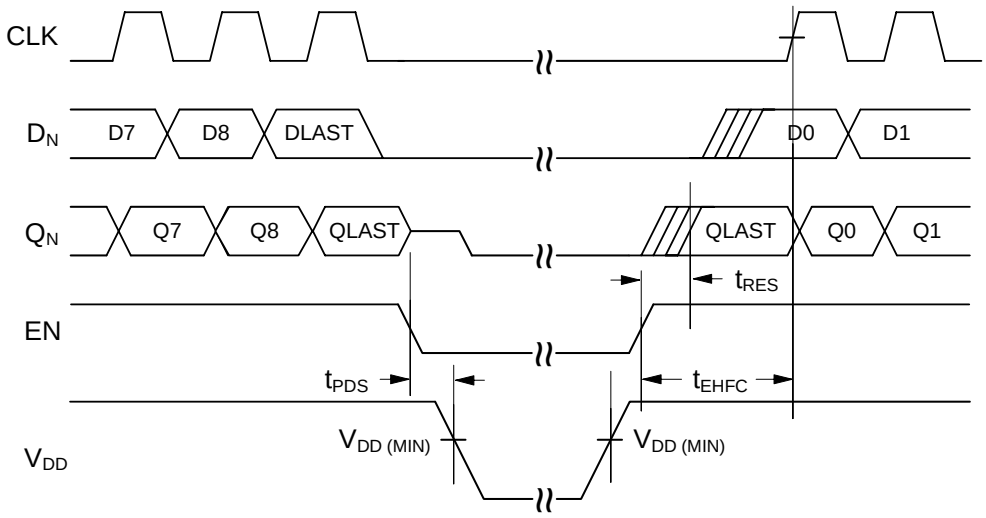
AC Test Conditions

Input Pulse Levels	0.1 V_{DD} to 0.9 V_{DD}
Input Rise and Fall Times	10 ns
Input and Output Timing Levels	0.5 V_{DD}
Output Load Capacitance	30pF

FM1110 Signal Timing

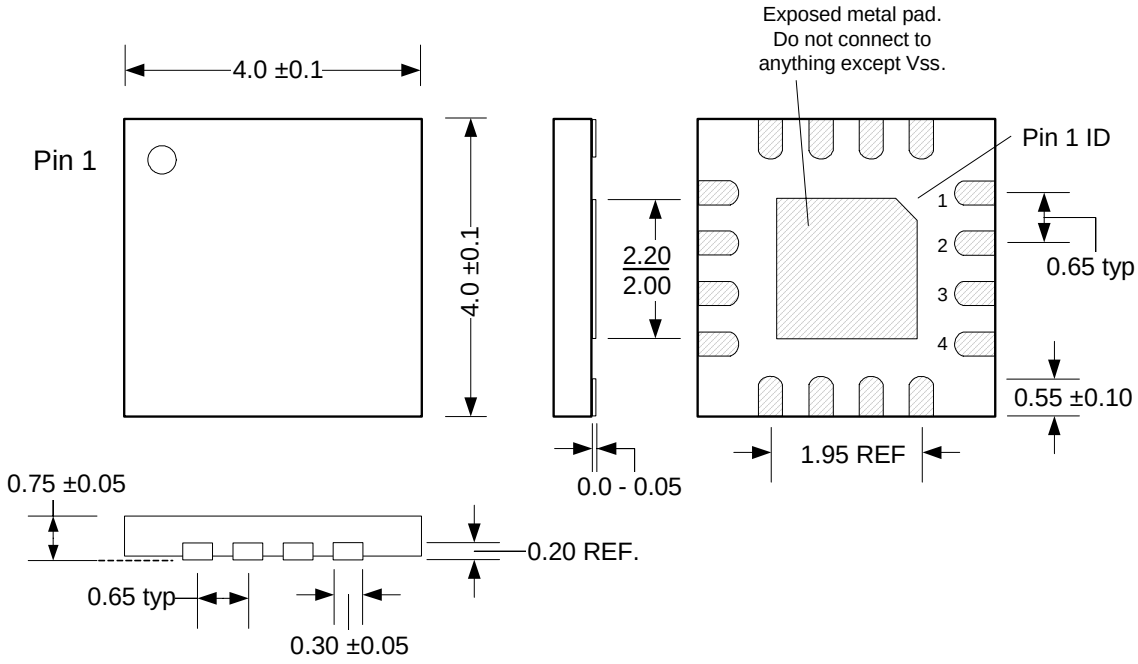


Power Cycle Timing



Mechanical Drawing

16-pin QFN (4.0mm x 4.0mm body, 0.65mm pitch)



Note: All dimensions in millimeters. **Care must be taken to ensure PCB traces and vias are not placed within the exposed metal pad area.**

QFN Package Marking Scheme

Legend:
XXXX=base part number, PP=package designator (Q=QFN, G="green")
LLLLLL= lot code
YY=year, WW=work week

Example: FM1110, "Green" QFN package, Lot 0001, Year 2007, Work Week 32

```
1110QG
0001
0732
```

Revision History

Revision	Date	Summary
1.0	8/8/2007	Initial Release.
2.0	2/20/2008	Changed to Pre-Production status. Changed V_{HYS} and t_{EHD} (min.) limits.